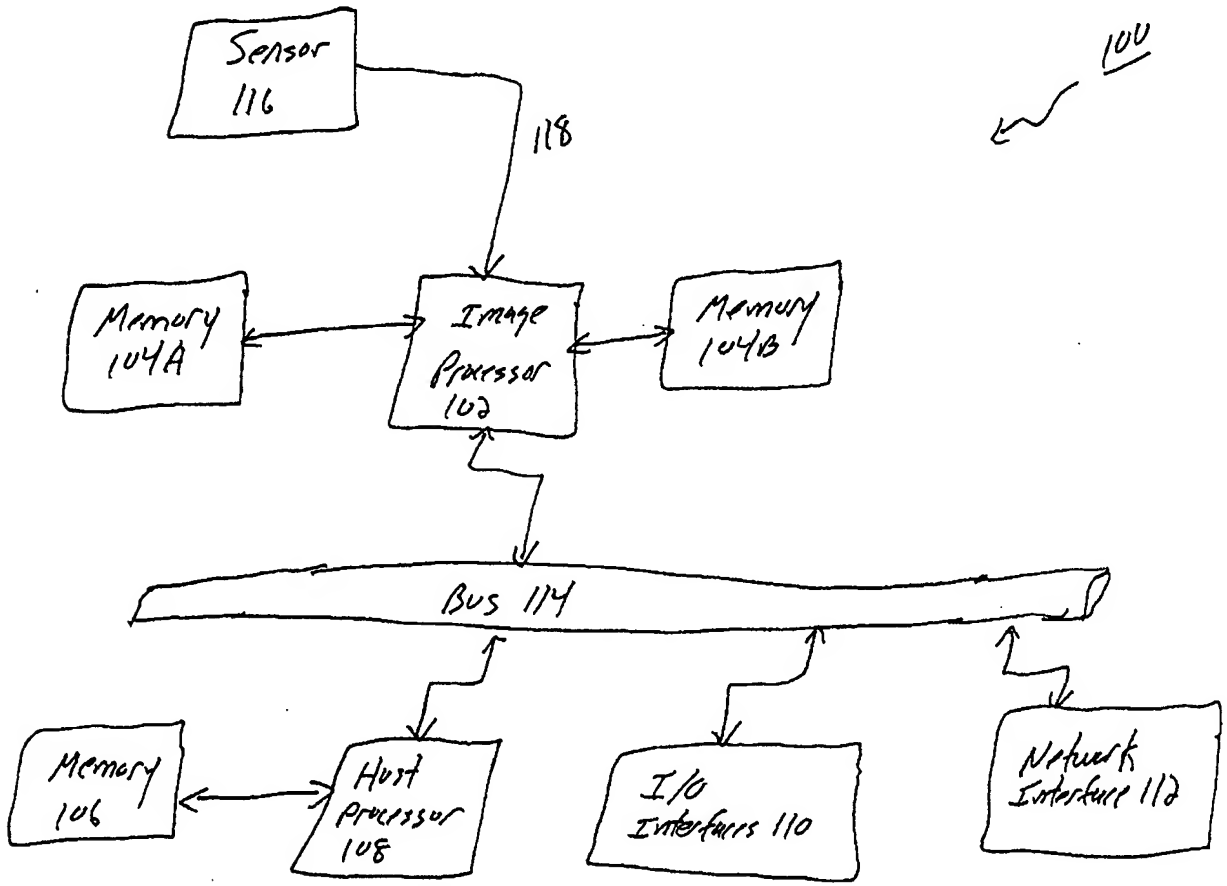
Sensor
116
118
100
Memory
104A
Image
Processor
102
Memory
104B
Bus 114
Memory
106
Host
Processor
108
I/O
Interfaces 110
Network
Interface 112

FIG 1

IMAGE PROCESSOR 100
MEMORY 104B
MEMORY INTERFACE 206B
DMA UNIT 204B
MEMORY INTERFACE 206A
DMA UNIT 204A
MEMORY 104A
210
212
208C
208A
208B
208D
208E
208F
208G
208H
206C
206A
206B
206D
206E
206F
206G
206H
204C
204A
204B
204D
204E
204F
204G
204H
202C
202A
202B
202D
202E
202F
202G
202H

FIG. 2

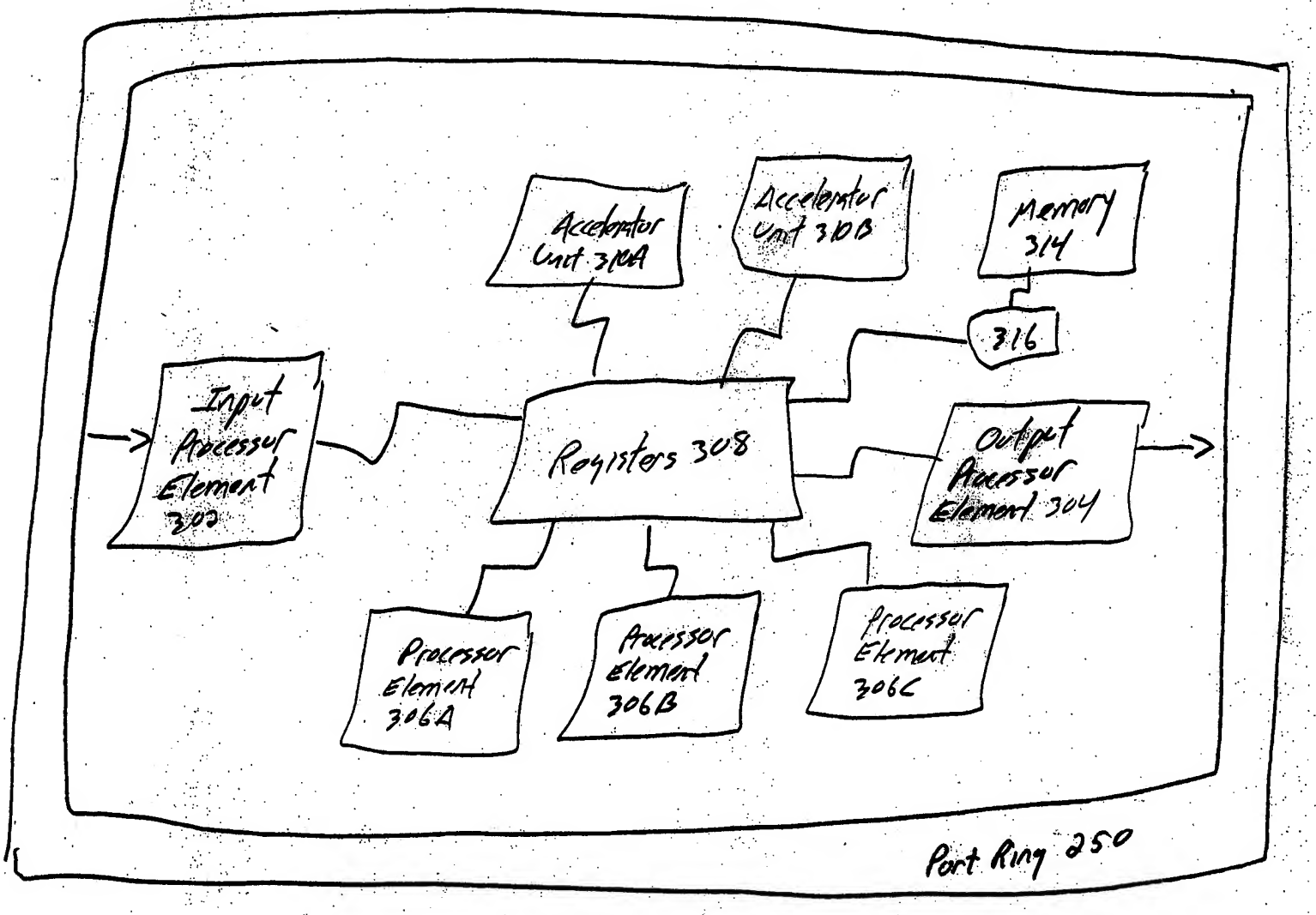
Accelerator Unit 310A
Accelerator Unit 310B
Memory 314
316
Input Processor Element 302
Registers 308
Output Processor Element 304
Processor Element 306A
Processor Element 306B
Processor Element 306C
Port Ring 250

FIG 3

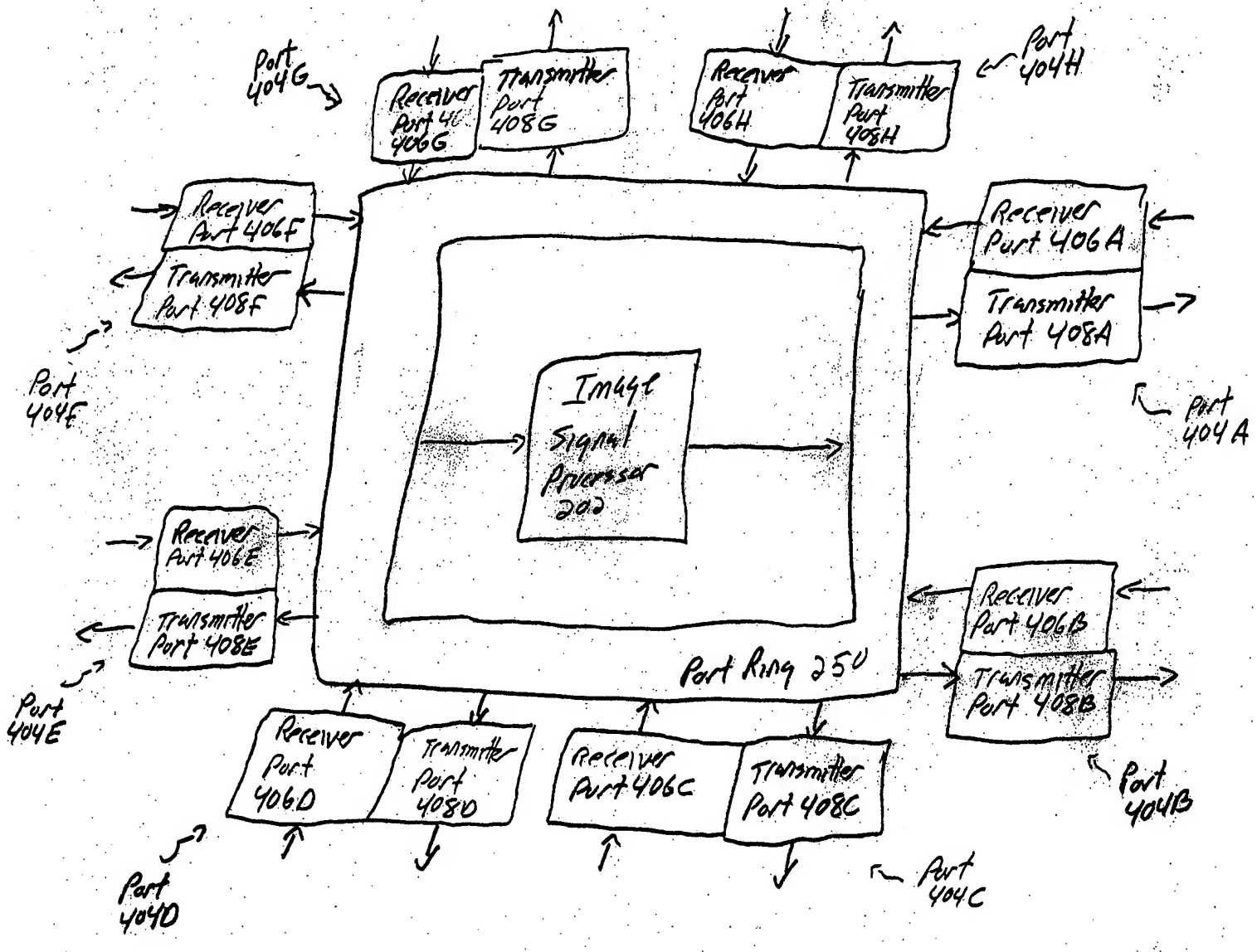
Port 404G
Receiver Port 406G
Transmitter Port 408G
Receiver Port 406H
Transmitter Port 408H
Port 404H
Receiver Port 406F
Transmitter Port 408F
Port 404F
Receiver Port 406A
Transmitter Port 408A
Port 404A
Image Signal Processor 202
Receiver Port 406E
Transmitter Port 408E
Port 404E
Port Ring 250
Receiver Port 406B
Transmitter Port 408B
Port 404B
Receiver Port 406D
Transmitter Port 408D
Port 404D
Receiver Port 406C
Transmitter Port 408C
Port 404C

FIG. 4

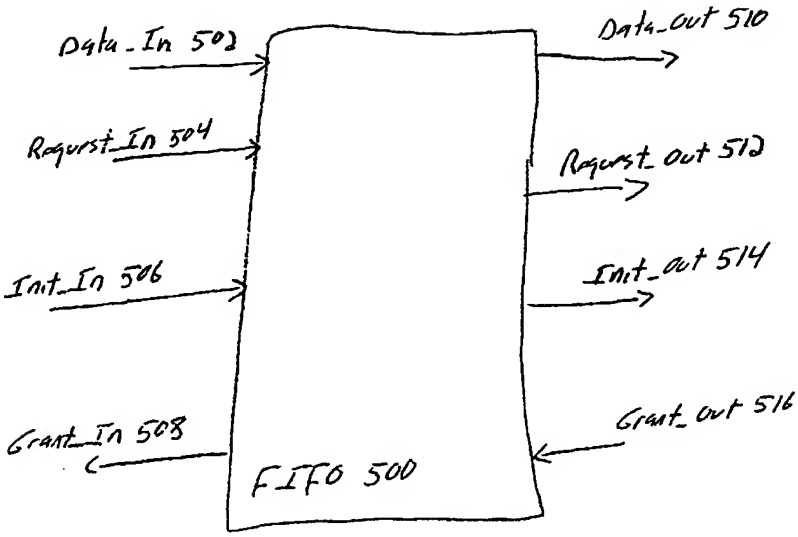
Data_In 502
Request_In 504
Init_In 506
Grant_In 508
FIFO 500
Data_out 510
Request_out 512
Init_out 514
Grant_out 516

FIG. 5

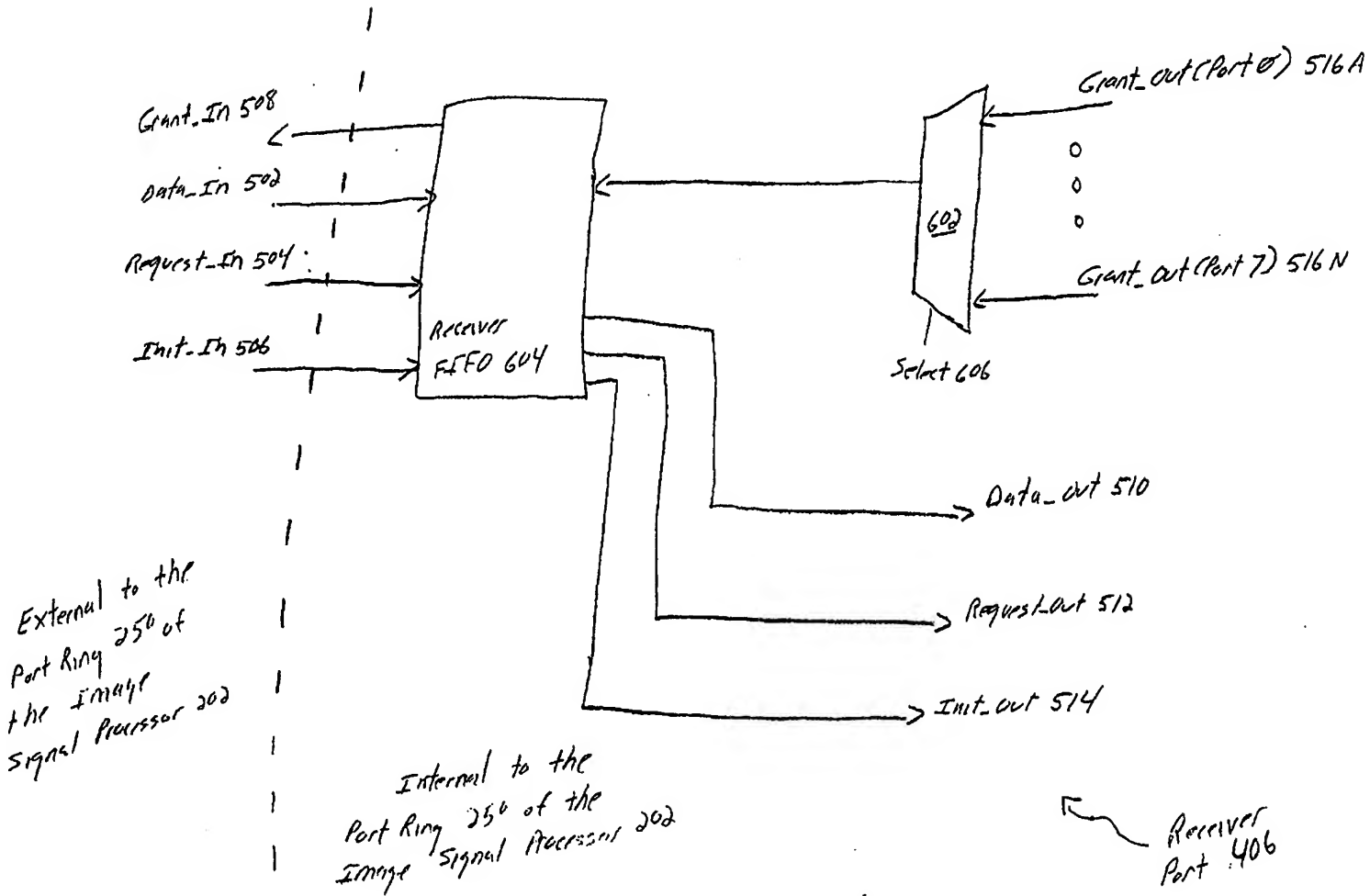
Grant_In 508
Data_In 502
Request_In 504
Init_In 506
Receiver FIFO 604
602
Grant_out (Port 0) 516A
Grant_out (Port 7) 516N
Select 606
Data_out 510
Request_out 512
Init_out 514
External to the Port Ring 256 of the Image Signal Processor 202
Internal to the Port Ring 256 of the Image Signal Processor 202
Receiver Port 406

FIG. 6

Init-IN signal 506
Init-OUT signal 514
Transmitter Port 408A
Receiver Port 408
Transmitter Port 408B
Base Unit 502A
DCD A
Base Unit 502B
DCD B

FIG 7A

Port Ring 350A
DOA
Transmitter Port 408A
Request-In Signal
Receiver Port 406
Transmitter Port 408B
Port Ring 350B
DOB

FIG 7B

Port Pwr 350A
Core A
Transmitter Port 406A
Grant-In Signal 508
Receiver Port 406
Transmitter Port 406B
Port Pwr 350B
Core B

FIG 7C

Port Plug 250A
Data
Transmitter Part 408A
Receiver Part 406
Data-In Signals 502
Transmitter Part 408B
Port Plug 250B
Data

FIG 7D

202A
Port Ring 250A
Transmitter Port 408A
Receiver Port 406
Request out Signal 512
Transmitter Port 408B
202B
Port Ring 250B

FIG 7E

Port Ring 250A
DOA A
Transmitter Port 408A
Receiver Port 406
Circuit-Out Signal 516
Transmitter Port 408B
Port Ring 250B
DOA B

FIG 7F

Port Ring 350A
302A
Transmitter Port 408A
Receiver Port 406
Data-out Signal 510
Transmitter Port 408B
302B
Port Ring 350B

FIG 7G

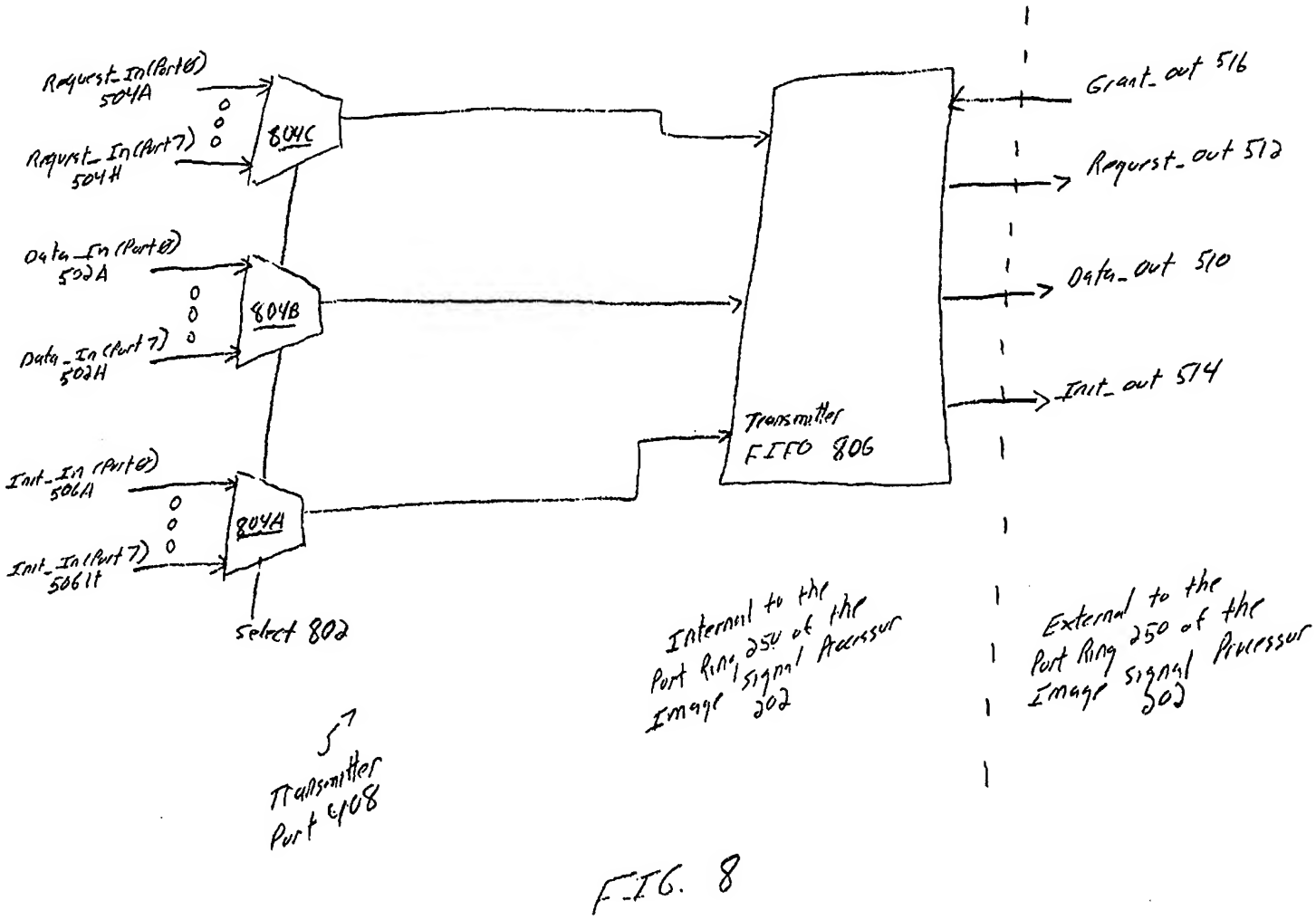
Request_In (Port 0) 504A
Request_In (Port 7) 504H
804C
Data_In (Port 0) 502A
Data_In (Port 7) 502H
804B
Init_In (Port 0) 506A
Init_In (Port 7) 506H
804A
Select 802
Transmitter FIFO 806
Grant_out 516
Request_out 512
Data_out 510
Init_out 514
Internal to the Port Ring 250 of the Image signal Processor 202
External to the Port Ring 250 of the Image signal Processor 202
Transmitter Port 408

FIG. 8

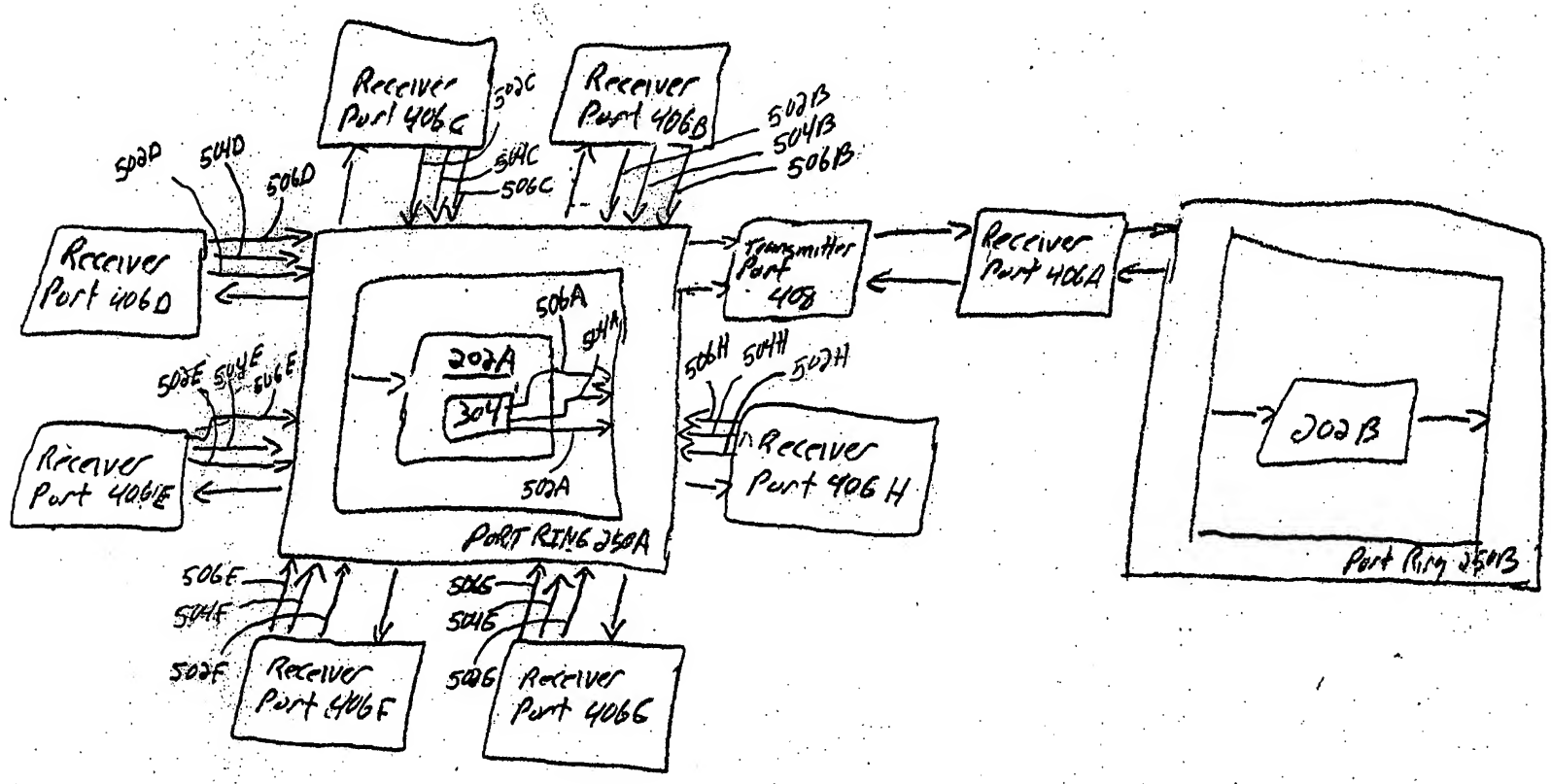
Receiver Port 406C
Receiver Port 406B
Receiver Port 406D
Receiver Port 406E
Receiver Port 406F
Receiver Port 406G
Receiver Port 406H
Transmitter Port 408
Receiver Port 406A
202A
304
202B
Port Ring 350A
Port Ring 350B
502A
502B
502C
502D
502E
502F
502G
502H
504A
504B
504C
504D
504E
504F
504G
504H
506A
506B
506C
506D
506E
506G
506H

FIG 9A

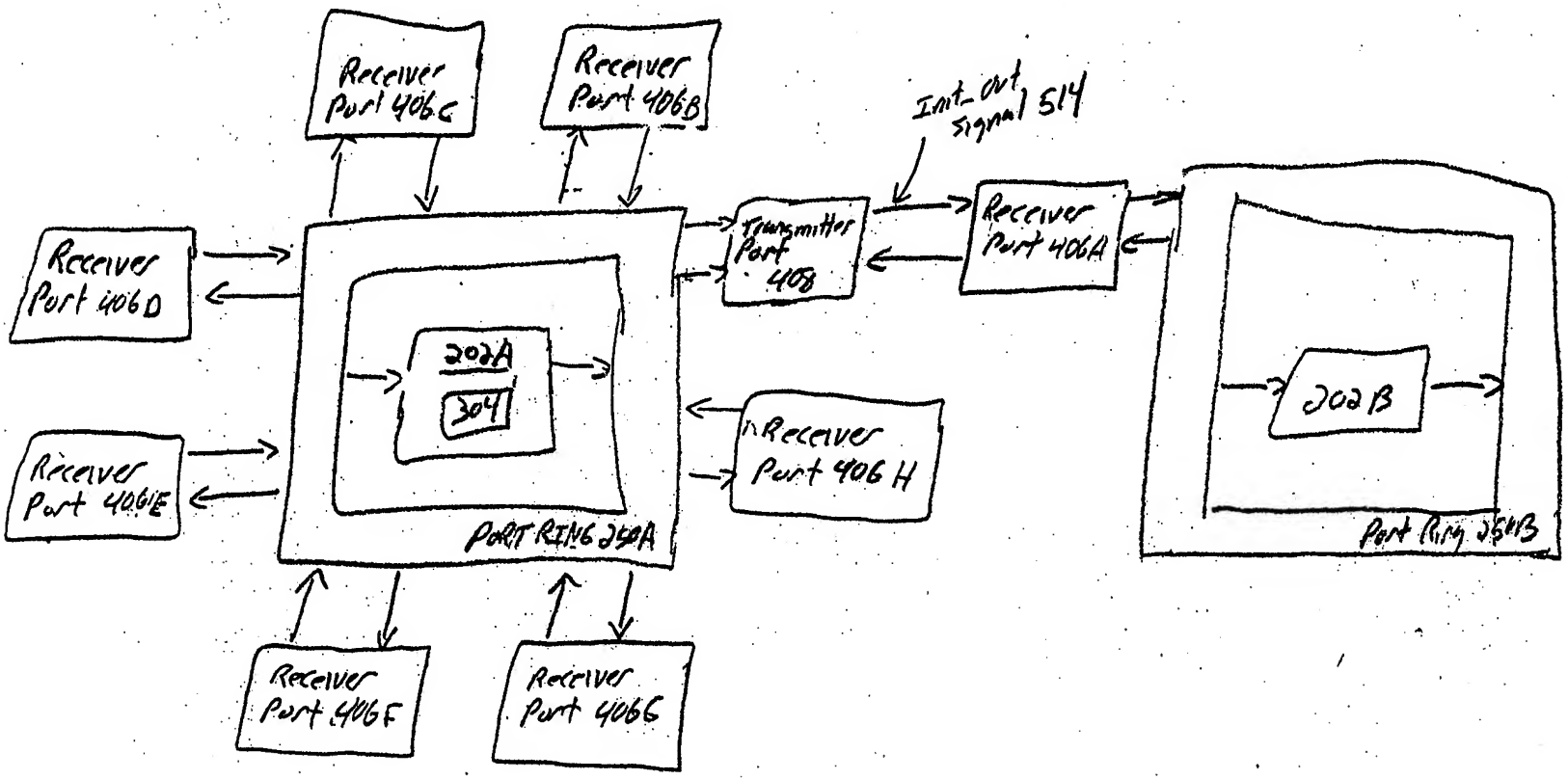
Receiver Port 406C
Receiver Port 406B
Init_Ort signal 514
Receiver Port 406D
Transmitter Port 408
Receiver Port 406A
202A
304
202B
Receiver Port 406E
Receiver Port 406H
PORT RING 250A
Port Ring 250B
Receiver Port 406F
Receiver Port 406G

FIG 9B

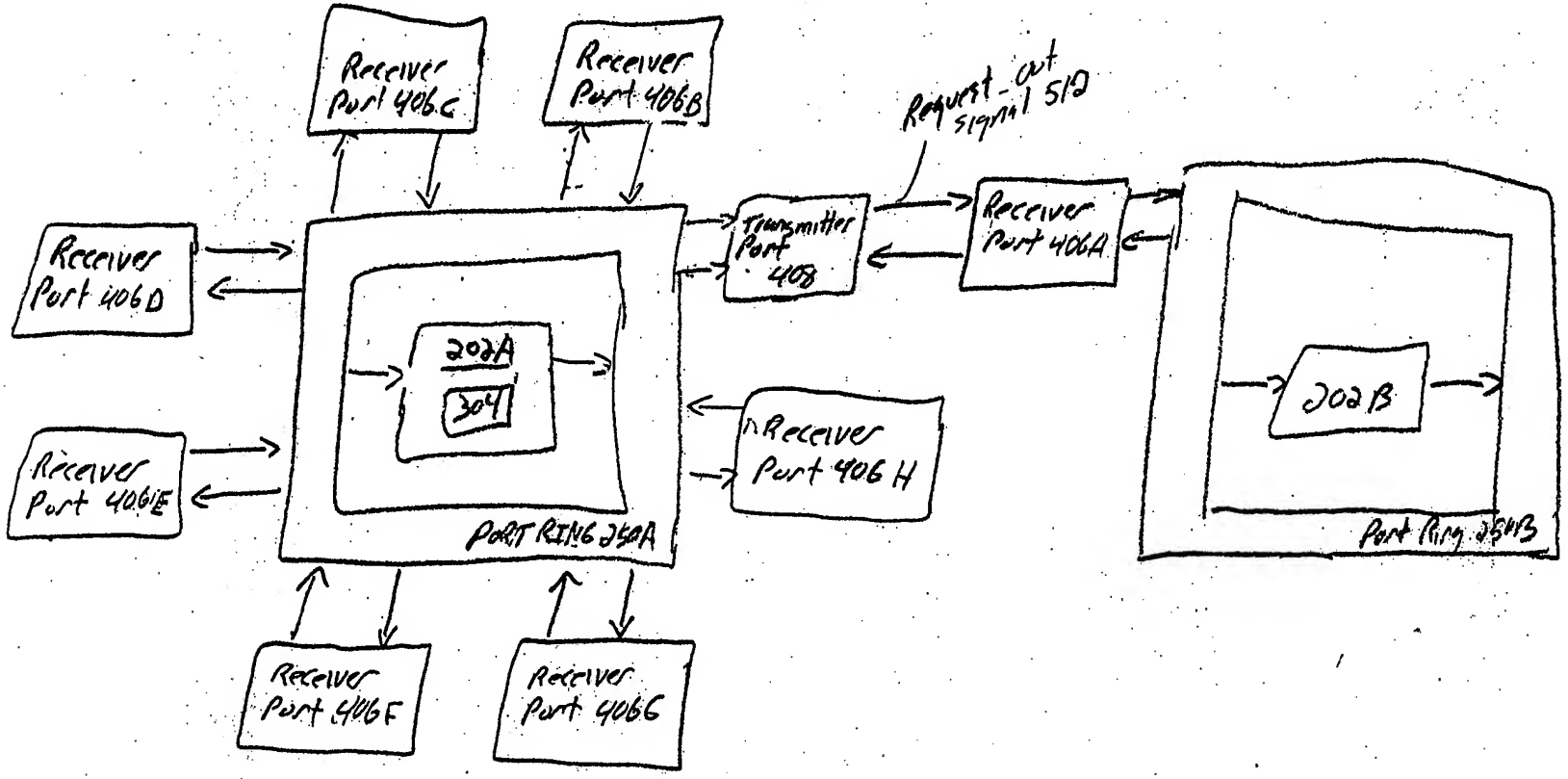
Receiver Port 406C
Receiver Port 406B
Request-out signal 512
Receiver Port 406D
Transmitter Port 408
Receiver Port 406A
202A
304
202B
Receiver Port 406E
Receiver Port 406H
PORT RING 350A
Port Ring 350B
Receiver Port 406F
Receiver Port 406G

FIG 9C

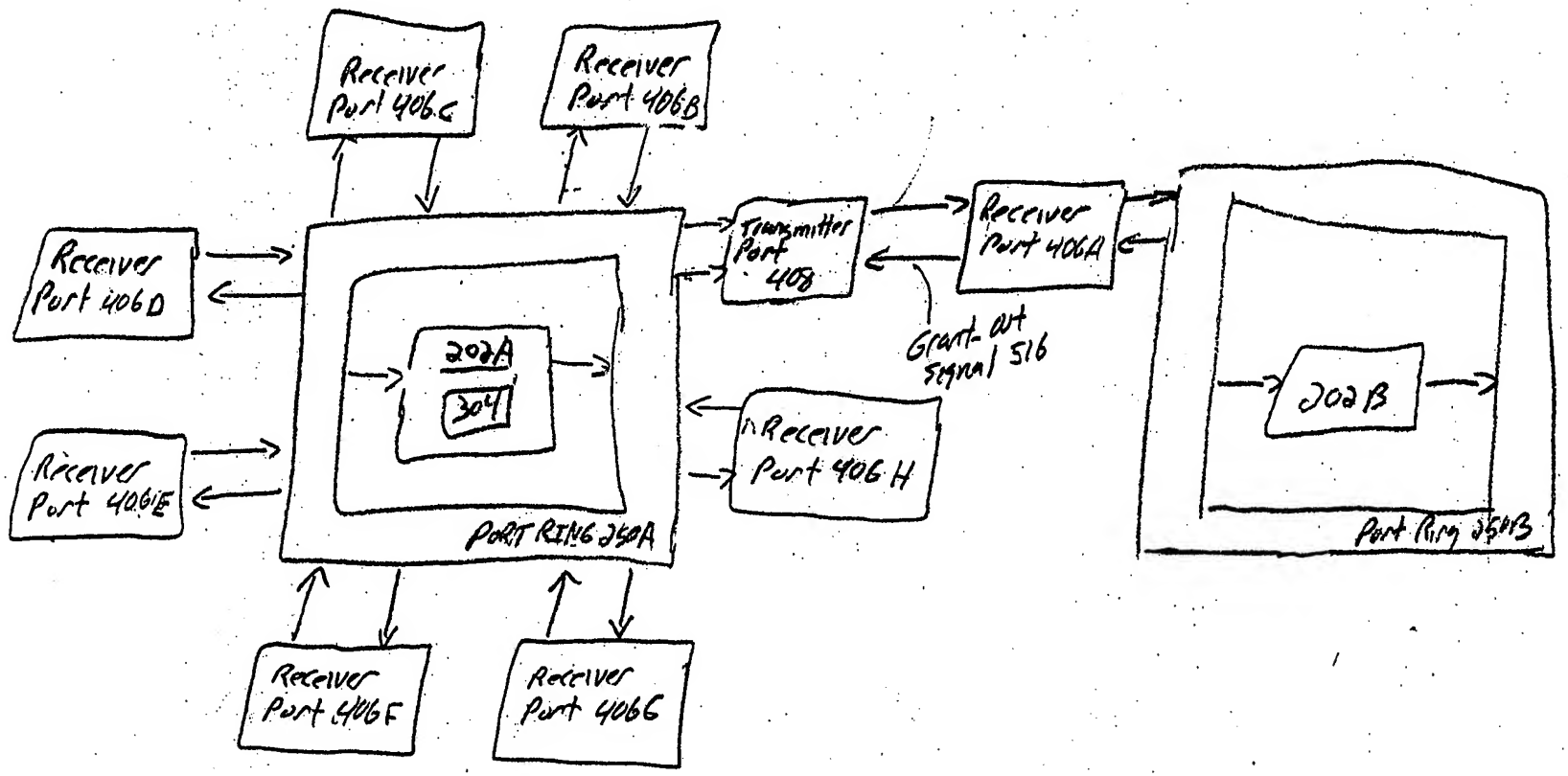
Receiver Port 406C
Receiver Port 406B
Receiver Port 406D
Transmitter Port 408
Receiver Port 406A
Grant-out signal 516
202A
304
202B
Receiver Port 406E
Receiver Port 406H
PORT RING 350A
PORT RING 350B
Receiver Port 406F
Receiver Port 406G

FIG 9D

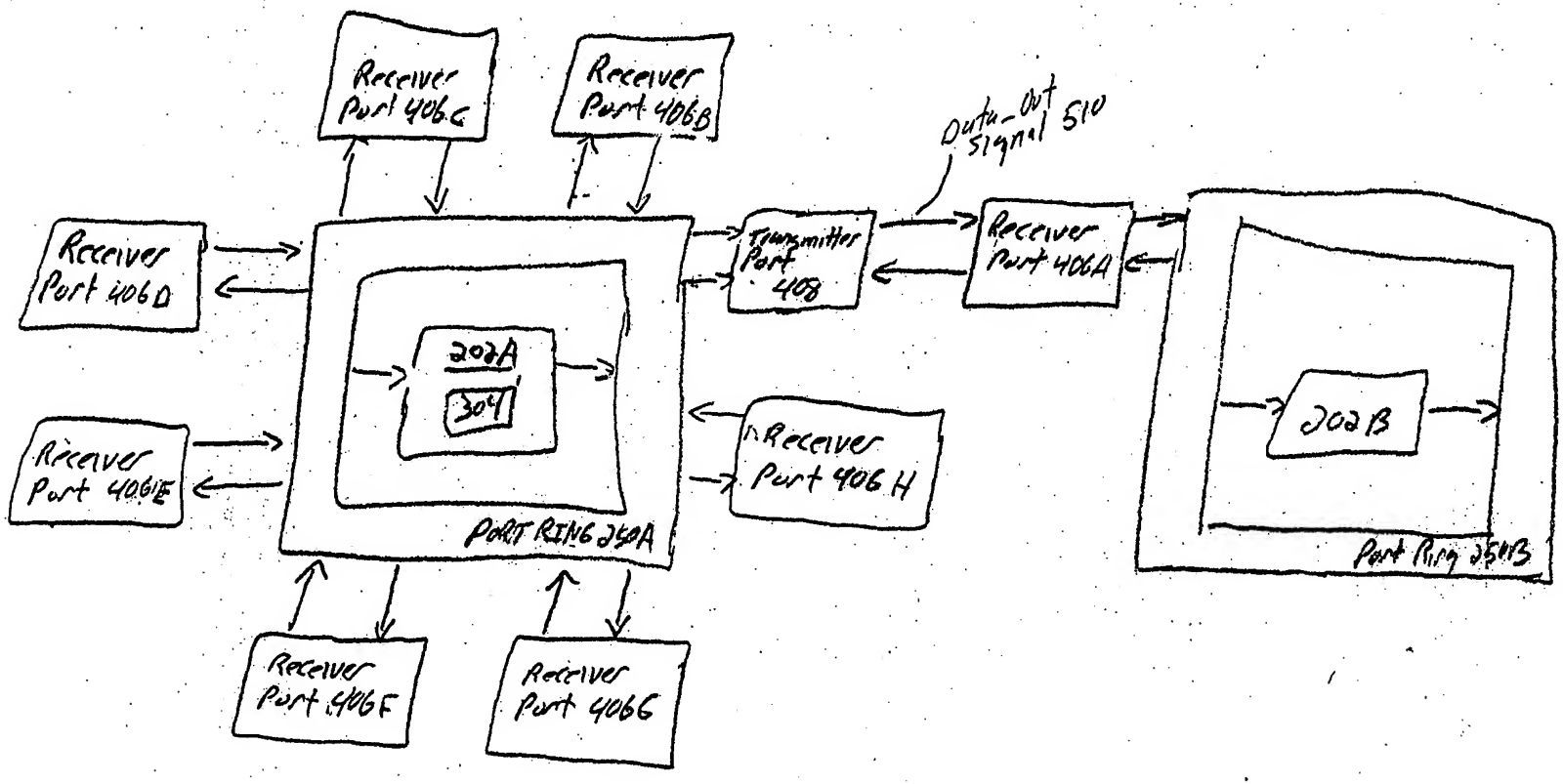
Receiver Port 406C
Receiver Port 406B
Data_Out signal 510
Receiver Port 406D
Transmitter Port 408
Receiver Port 406A
202A
304
202B
Receiver Port 406E
Receiver Port 406H
PORT RING 250A
Port Ring 250B
Receiver Port 406F
Receiver Port 406G

FIG 9E

IMAGE PROCESSOR 102
MEMORY 104B
MEMORY INTERFACE 206B
DMA UNIT 204B
MEMORY 104A
MEMORY INTERFACE 206A
DMA UNIT 204A
CPU 210
GPU 208
100A
100B
100C
100D
100E
100F
100G
100H
100I
100J
100K
100L
100M
100N
100O
100P
100Q
100R
100S
100T
100U
100V
100W
100X
100Y
100Z

FIG. 10

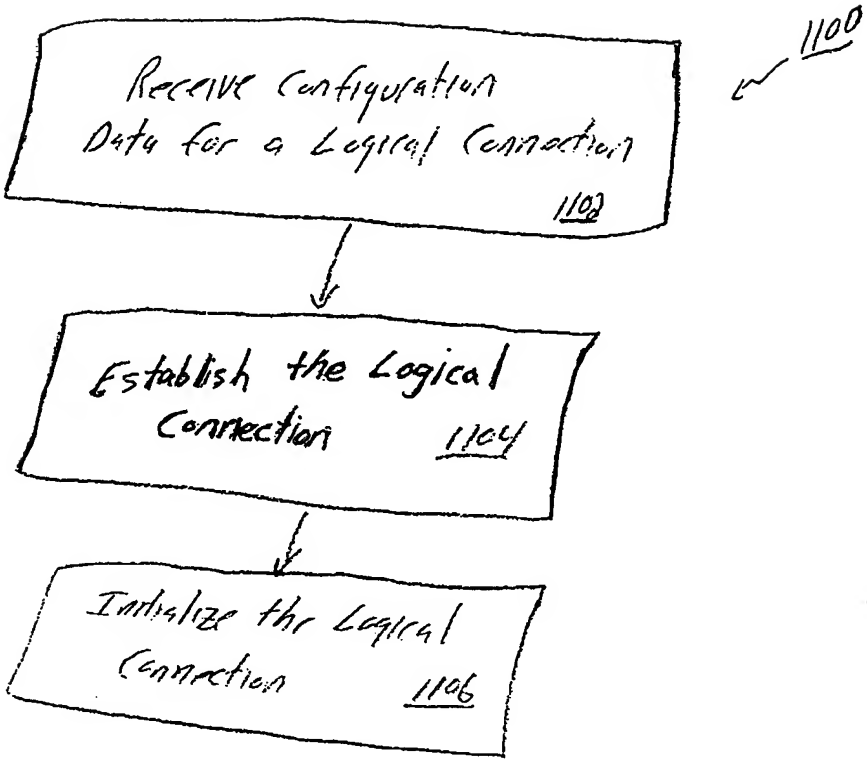
1100
Receive Configuration Data for a Logical Connection
1102
Establish the Logical Connection
1104
Initialize the Logical Connection
1106

FIG. 11

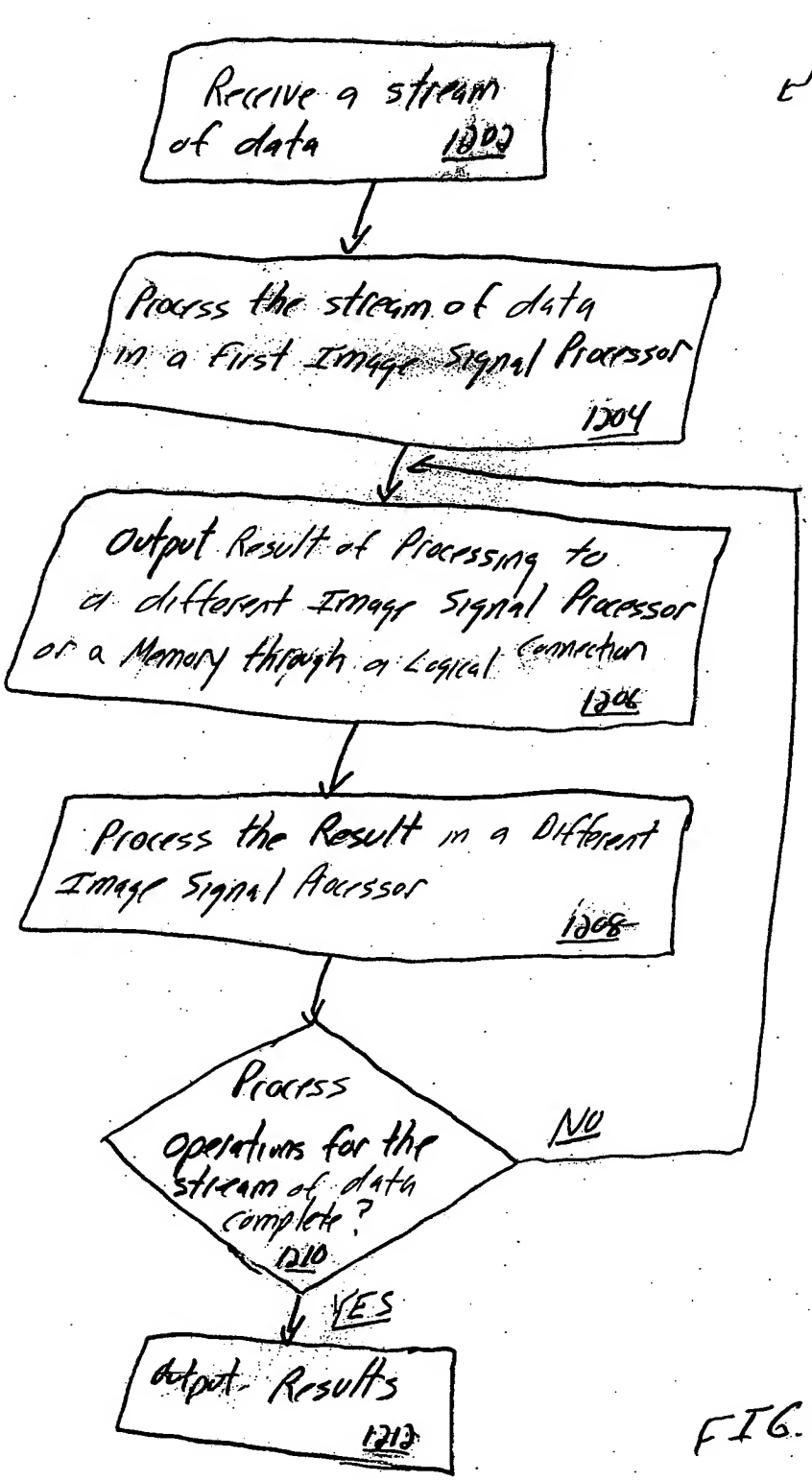
1200
Receive a stream of data 1202
Process the stream of data in a first Image Signal Processor 1204
Output Result of Processing to a different Image Signal Processor or a Memory through a Logical Connection 1206
Process the Result in a Different Image Signal Processor 1208
Process Operations for the stream of data complete? 1210
NO
YES
Output Results 1212

FIG. 12

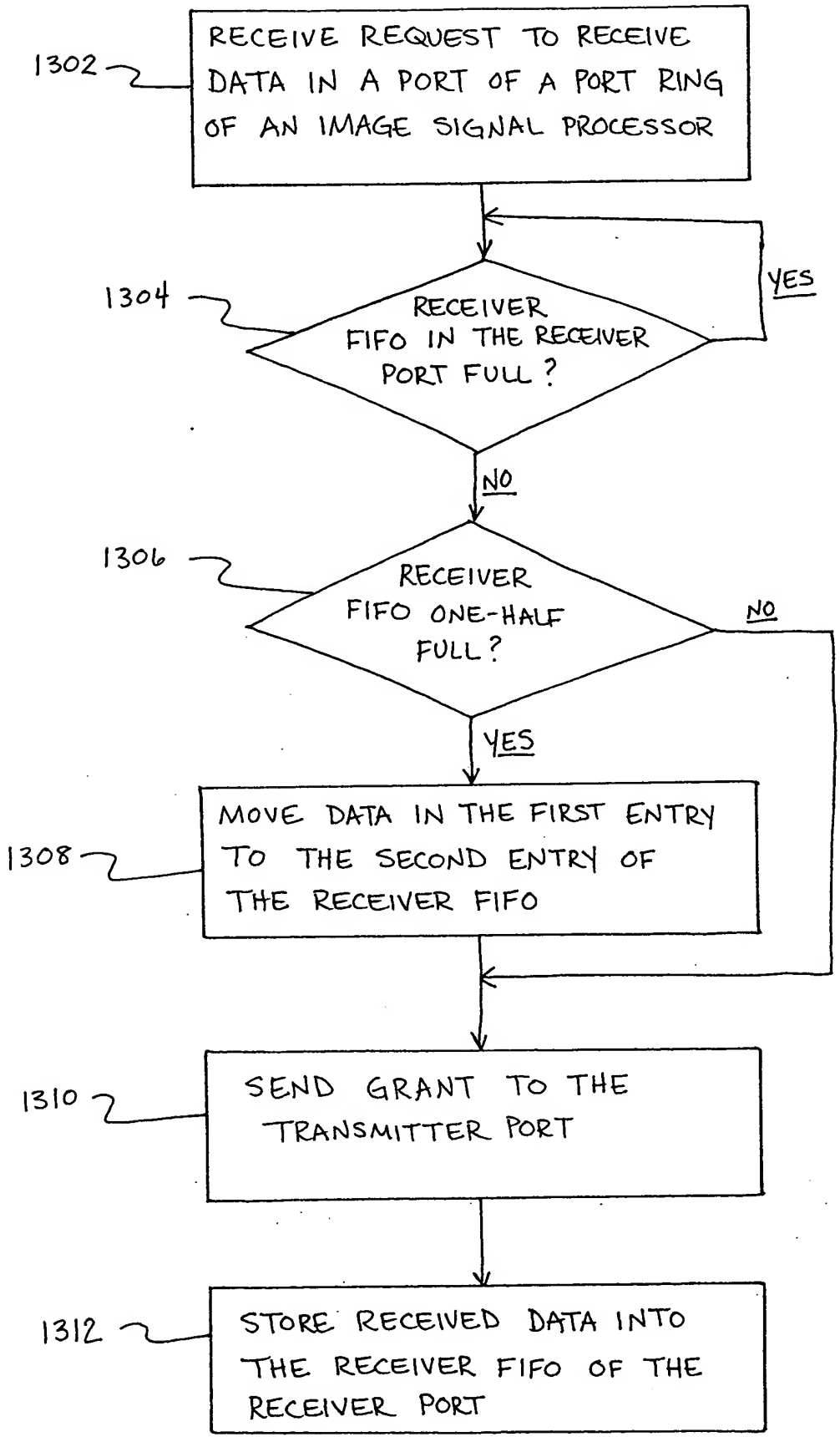
1300
1302
RECEIVE REQUEST TO RECEIVE DATA IN A PORT OF A PORT RING OF AN IMAGE SIGNAL PROCESSOR
1304
RECEIVER FIFO IN THE RECEIVER PORT FULL ?
YES
NO
1306
RECEIVER FIFO ONE-HALF FULL ?
NO
YES
1308
MOVE DATA IN THE FIRST ENTRY TO THE SECOND ENTRY OF THE RECEIVER FIFO
1310
SEND GRANT TO THE TRANSMITTER PORT
1312
STORE RECEIVED DATA INTO THE RECEIVER FIFO OF THE RECEIVER PORT

FIG. 13A

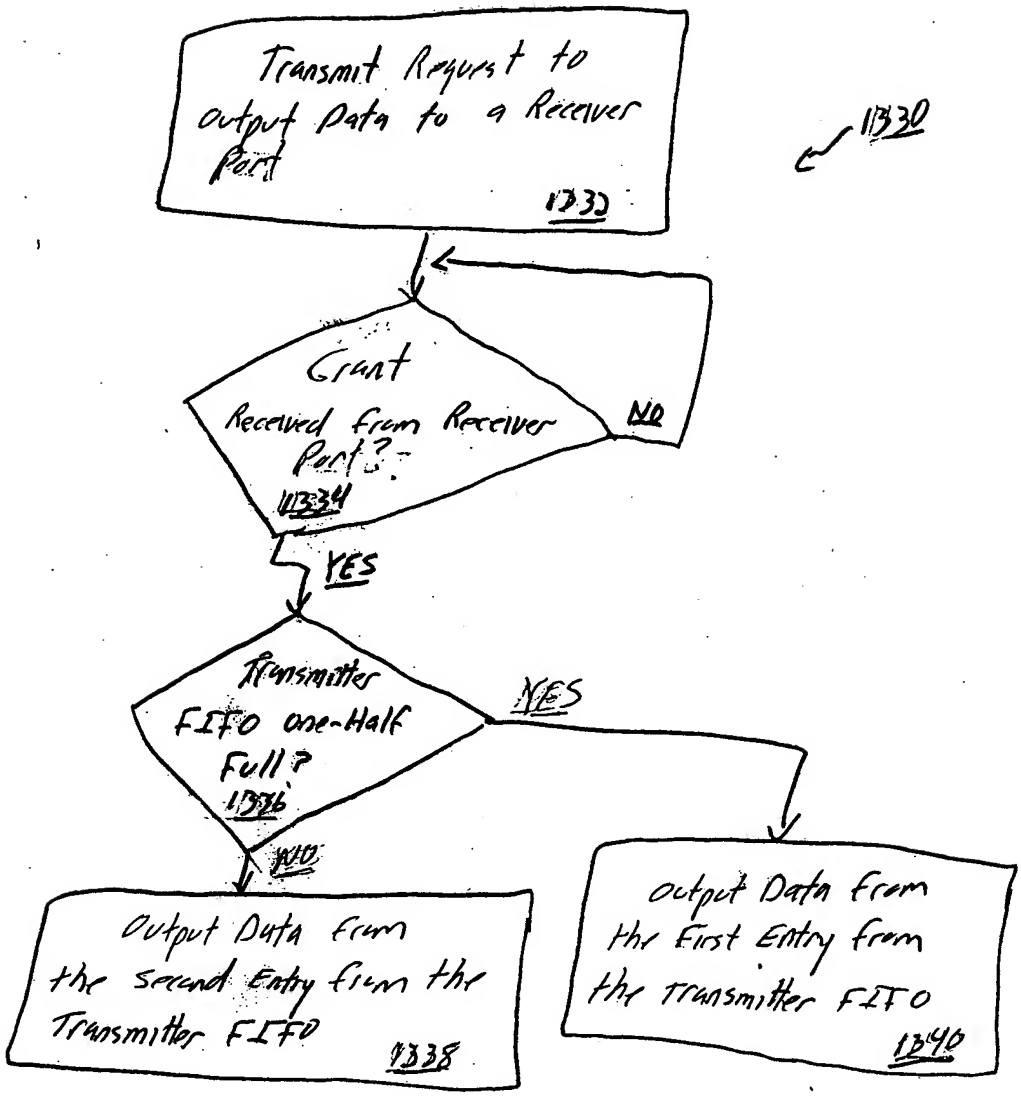
Transmit Request to output Data to a Receiver Part
1332
1330
Grant Received from Receiver Part?
1334
NO
YES
Transmitter FIFO one-Half Full?
1336
YES
NO
Output Data from the First Entry from the Transmitter FIFO
1340
Output Data from the second Entry from the Transmitter FIFO
1338

FIG. 13B

Memory 106
Host Processor 108
Bus 114
I/O Interface 110
Network Interface 112
Sensor 116
118
Image Processor 102A
Memory 104A
Memory 104B
Image Processor 102B
Memory 104C
Image Processor 102N
Memory 104N
Memory 104F
Image Processor 102H
Memory 104H

FIG. 14

1400